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10/541,373	06/29/2005	Masayuki Koga	YKI-0181	1081

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CANTOR COLBURN, LLP
20 Church Street
22nd Floor
Hartford, CT 06103

EXAMINER	
RAINEY, ROBERT R	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/541,373	KOGA ET AL.	
	Examiner	Art Unit	
	Robert R. Rainey	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-19* is/are allowed.

6)☒ Claim(s) *1, 4-7, and 10-14* is/are rejected.

7)☒ Claim(s) *1-3, 8, 9, 12, 15, and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 6/29/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore:

The "first power source" recited in **claims 1, 12 and 16** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

The four connections to the correction transistor claimed in **claims 15 and 16** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Both claims claim "a correction transistor having a control end connected to a first power source at a predetermined voltage, a first conductive region connected to a second conductive region of the selection transistor, and a second conducive region connected to a control end of the driving transistor". Claim 15 further claims "the correction transistor includes an active layer formed between the data line and the power source line to extend partially underlying at least one of these lines." While claim 16 further claims "at least part of an active layer of the correction transistor is formed below the power source line with an insulating layer disposed in between". Thus both claims require at least four connections to be shown. Further, connection of the correction transistor to the

data line is nowhere shown but falls within the scope of claim 15 and thus must be shown or canceled from the claim.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. Figure 13 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled

"Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to because the claims recite a "pulse voltage line" the corresponding term used in the drawings is "SC". The inconsistent use of terminology between the claims and the drawings is unnecessarily confusing. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Regarding **claim 15**, the connections claimed for the correction transistor are not supported by the specification. In the first instance is recited in the parent claim, claim 12: "a correction transistor having a control end connected to a first power source at a predetermined voltage, a first conductive region connected to a second conductive region of the selection transistor, and a second conducive region connected to a control end of the driving transistor". And in the second instance: "the correction transistor includes an active layer formed between the data line and the power source line to extend partially underlying at least one of these lines." In the first instance the correction transistor is not connected to the power source line but to a separate "first power source" nor is it connected to the data line. In the second instance the correction transistor is connected to the power source line or to the data line. Such connection would require a four terminal device, which is nowhere disclosed. Further, connection of the correction transistor to the data line is nowhere disclosed but falls within the scope of the claim.

Regarding **claim 16**, the connections claimed for the correction transistor are not supported by the specification. In the first instance is recited: "a correction transistor having a control end connected to a first power source at a predetermined voltage, a first conductive region connected to a second conductive region of the selection transistor, and a second conductive region connected to a control end of the driving transistor". And in the second instance: "at least part of an active layer of the correction transistor is formed below the power source line with an insulating layer disposed in between." In the first instance the correction transistor is not connected to the power source line but to a separate "first power source". In the second instance the correction transistor is connected to the power source line. Such connection would require a four terminal device, which is nowhere disclosed.

Claim Objections

5. **Claims 1, 12 and 16** objected to because of the following informalities:

Regarding **claim 1**, the phrase "... the correction transistor is switched on and off states ..." is unclear as written but seems to indicate that "... the correction transistor is switched between on and off states ..." or with the same meaning but even more clearly stated "... the correction transistor is switched from an on to an off state ...".

Regarding **claims 12 and 16**, in the phrase "the voltage of the control end when the driving transistor turns on" it is unclear which "control end" is meant since control ends of three different transistors are cited. Since the control end of the driving transistor was most recently mentioned it seems most likely that this is the one meant and could be made clear by referring explicitly to it: "the voltage of the control end of the driving transistor when the driving transistor turns on"

Regarding **claims 12 and 16**, there seems to be an error in the phrase "and a second conducive region connected to a control end of the driving transistor" in that the word "conducive" was inadvertently inserted for the word "conductive".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. **Claims 5 and 11** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding **claims 5 and 11**, the phrase "... laser irradiated upon the polycrystallization laser annealing..." is unclear. It is unclear how the laser can irradiate a process.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 4 rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,359,605 to *Knapp et al.* ("*Knapp*").

As to **claim 1**, *Knapp* discloses a pixel circuit, comprising: a selection transistor (see for example Fig. 3 item 34) having one end connected to a data line (see for example Fig. 3 item 14), and a control end receiving a selection signal (see for example Fig. 3 item 12); a correction transistor (see for example Fig. 3 item 32) having one end connected to the other end of the selection transistor, and a control end connected to a first power source at a predetermined voltage (see for example Fig. 3 in which the voltage is predetermined as indicated in the upper right of the figure); a driving transistor (see for example Fig. 3 item 24) having a control end connected to the other end of the correction transistor, and one end connected to a second power source (see for example Fig. 3 item 22) functioning as a current supply source (Since

any power source in the context of an electronic device supplies current, the phrase "functioning as a current supply source" adds no additional patentable weight.); a storage capacitor (see for example Fig. 3 item 30) having one end connected to the control end of the driving transistor, and the other end connected to a pulse voltage line (see for example Fig. 3 item 28 labeled VS2 and column 7 lines 31-36, which state that VS2 may be the next or previous row conductor line; noting that the row conductor lines provide a pulse voltage); and an emissive element (see for example Fig. 3 item 20) for emitting light caused by a current flowing through the driving transistor, wherein the correction transistor is switched on and off states (see for example Fig. 3, noting that transistor 32 is turned of either by the fall of the voltage on line 12 from VS to VL or by the rise of the voltage on line 28 from VL to VS depending on which occurs first) in a process of turning on the driving transistor (the voltage pulses on lines 12 and 28 occur in the process of turning on the driving transistor) by changing a voltage value of the pulse voltage line (see for example column 7 lines 41-45, noting that the row driver must be capable of supplying, i.e. sinking, the drive current for the display elements in the row it serves in its low level state, so in its high level state it does not need to sink the current, which means that transistors 24 are off), thereby controlling a voltage of the control end of the driving transistor when it is turned on (when line 28 drops from VS to VL transistor 24 turns on and the voltage at its control end is that set by the interaction of the disclosed transistors and control signals), and the driving transistor and the correction transistor are

formed adjacent to each other (see for example Fig. 1 items 10 and column 5 lines 14-15, which describe item 10 as comprising electroluminescent display elements together with associated switching means, which are represented by Fig. 3, thus the transistors are within the boundaries of item 10 and thus adjacent to each other; or see for example column 2 lines 65-67).

As to **claim 4**, in addition to the rejection of claim 1 *Knapp* further discloses that the correction transistor and the driving transistor are p-channel transistors (see for example column 8 lines 65-66), and the pulse voltage line changes from a high level to a low level after the selection transistor is turned off (see for example Fig. 3 item 28 labeled VS2 and column 7 lines 31-36, which state that VS2 may be the next or previous row conductor line; noting that the row conductor lines provide a pulse voltage after the selection transistor is turned off).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 5 and 11-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,359,605 to *Knapp et al.* ("*Knapp*") in view of U.S. Patent No. 6,812,491 to *Kato et al.* ("*Kato*").

As to **claim 5**, in addition to the rejection of claim 1 over *Knapp*:

Knapp does not expressly disclose that active layers of the correction transistor and the driving transistor are formed of polycrystalline semiconductor obtained by polycrystallization laser annealing, and a channel length direction of the correction transistor and a channel length direction of the driving transistor are disposed in parallel to a scanning direction of a line-shaped pulse laser irradiated upon the polycrystallization laser annealing, and at least part of both channel regions of the correction transistor and the driving transistor are located on the same line extending in a direction crossing the scanning direction of the pulse laser.

Kato discloses a thin film transistor and in particular: active layers of the transistor formed of polycrystalline semiconductor obtained by polycrystallization laser annealing, and a channel length direction of the transistor disposed in parallel to a scanning direction of a line-shaped pulse laser irradiated upon the polycrystallization laser annealing (see for example column 6 lines 30-43).

Examiner takes official notice that it was well known to those skilled in the art at the time of the invention that the more similar the manufacturing conditions of semiconductor devices the more similar their properties will be. As evidence of this one can see for example *Knapp* column 2 lines 65-67 that states that

transistors manufactured close to each other will have similar characteristics. As further evidence one can note the expansion of the Toyota Manufacturing system and statistical process control in general with its emphasis on reducing manufacturing variation to a wide variety of manufacturing industries including semiconductor manufacturing.

Knapp and *Kato* are analogous art because they are from the same field of endeavor, which is thin film transistor based devices, and attempt to solve the same problem, which is to reduce the variability between thin film transistors.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to manufacture the transistors of *Knapp* with their channels aligned as disclosed by *Kato*. Thus *Knapp* and *Kato* disclose the claimed invention except for providing that at least part of both channel regions of the correction transistor and the driving transistor are located on the same line extending in a direction crossing the scanning direction of the pulse laser. It would have been obvious to one having ordinary skill in the art at the time the invention was made to so align the channel regions since it was known in the art that semiconductor devices formed under similar conditions, which includes the portions of the polycrystalline layer used for the channel regions of the two transistors being formed at the same time, exhibit similar properties. The suggestion/motivation would have been to provide advantages such as to provide better charge carrier mobility by reducing grain boundaries along the

length of the channels (see for example *Kato* column 6 lines 42-43) or to make the transistors more similar (see for example *Knapp* column 2 lines 66-67).

As to **claim 11**, in addition to the rejection of claim 6 over *Knapp*:

Knapp does not expressly disclose that active layers of the correction transistor and the driving transistor are formed of polycrystalline semiconductor obtained by polycrystallization laser annealing, and a channel length direction of the correction transistor and a channel length direction of the driving transistor are disposed in parallel to a scanning direction of a line-shaped pulse laser irradiated upon the polycrystallization laser annealing, and at least part of both channel regions of the correction transistor and the driving transistor are located on the same line extending in a direction crossing the scanning direction of the pulse laser.

Kato discloses a thin film transistor and in particular: active layers of the transistor formed of polycrystalline semiconductor obtained by polycrystallization laser annealing, and a channel length direction of the transistor disposed in parallel to a scanning direction of a line-shaped pulse laser irradiated upon the polycrystallization laser annealing (see for example column 6 lines 30-43).

Examiner takes official notice that it was well known to those skilled in the art at the time of the invention that the more similar the manufacturing conditions of semiconductor devices the more similar their properties will be. As evidence of this one can see for example *Knapp* column 2 lines 65-67 that states that

transistors manufactured close to each other will have similar characteristics. As further evidence one can note the expansion of the Toyota Manufacturing system and statistical process control in general with its emphasis on reducing manufacturing variation to a wide variety of manufacturing industries including semiconductor manufacturing.

Knapp and *Kato* are analogous art because they are from the same field of endeavor, which is thin film transistor based devices, and attempt to solve the same problem, which is to reduce the variability between thin film transistors.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to manufacture the transistors of *Knapp* with their channels aligned as disclosed by *Kato*. Thus *Knapp* and *Kato* disclose the claimed invention except for providing that at least part of both channel regions of the correction transistor and the driving transistor are located on the same line extending in a direction crossing the scanning direction of the pulse laser. It would have been obvious to one having ordinary skill in the art at the time the invention was made to so align the channel regions since it was known in the art that semiconductor devices formed under similar conditions, which includes the portions of the polycrystalline layer used for the channel regions of the two transistors being formed at the same time, exhibit similar properties. The suggestion/motivation would have been to provide advantages such as to provide better charge carrier mobility by reducing grain boundaries along the

length of the channels (see for example *Kato* column 6 lines 42-43) or to make the transistors more similar (see for example *Knapp* column 2 lines 66-67).

As to **claim 12**, *Knapp* discloses a display device including a plurality of pixels arranged in a matrix (see for example column 1 lines 6-7), each pixel comprising: a display element operating in accordance with supplied power (see for example column 1 lines 6-10); a selection transistor (see for example Fig. 3 item 34) having a first conductive region connected to a data line (see for example Fig. 3 item 14), and a control end receiving a selection signal (see for example Fig. 3 item 12); a driving transistor (see for example Fig. 3 item 24) having a first conductive region connected to a power source line (see for example Fig. 3 item 22) for supplying power to the display element (see for example Fig. 3 item 20); a correction transistor (see for example Fig. 3 item 32) having a control end connected to a first power source at a predetermined voltage (see for example Fig. 3 in which the voltage is predetermined as indicated in the upper right of the figure), a first conductive region connected to a second conductive region of the selection transistor (see for example Fig. 3), and a second conducive region connected to a control end of the driving transistor (see for example Fig. 3); and a storage capacitor (see for example Fig. 3 item 30) having a first electrode connected to the control end of the driving transistor and the second conductive region of the correction transistor, and a second electrode connected to a pulse voltage line (see for example Fig. 3 item 28 labeled VS2

and column 7 lines 31-36, which state that VS2 may be the next or previous row conductor line; noting that the row conductor lines provide a pulse voltage); wherein in accordance with an operation threshold thereof (without an operation threshold there would be no control), the correction transistor controls, in accordance with a change in a voltage of the control end of the driving transistor in response to a change in a voltage of the pulse voltage line, the voltage of the control end when the driving transistor turns on (when line 28 drops from VS to VL transistor 24 turns on and the voltage at its control end is that set by the interaction of the disclosed transistors and control signals), the correction transistor and the driving transistor are formed as transistors of the same conductivity type (see for example Fig. 3 or column 8 lines 65-66), and the channel regions thereof are disposed in close proximity to each other (see for example column 2 lines 66-67).

Knapp does not expressly disclose that at least a channel region of each of the correction transistor and the driving transistor is formed of a semiconductor layer polycrystallized through laser annealing.

Kato discloses a thin film transistor and in particular: at least a channel region of each transistor formed of a semiconductor layer polycrystallized through laser annealing (see for example column 6 lines 30-43).

Knapp and *Kato* are analogous art because they are from the same field of endeavor, which is thin film transistor based devices, and attempt to solve the same problem, which is to reduce the variability between thin film transistors.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to manufacture the transistors of *Knapp* with their channels made of a semiconductor layer polycrystallized through laser annealing as disclosed by *Kato*. The suggestion/motivation would have been to provide advantages such as to provide better charge carrier mobility by reducing grain boundaries along the length of the channels (see for example *Kato* column 6 lines 42-43).

As to **claim 13**, in addition to the rejection of claim 12 over *Knapp* and *Kato, Kato* further discloses a thin film transistor and in particular: active layers of the transistor formed of polycrystalline semiconductor obtained by polycrystallization laser annealing, and a channel length direction of the transistor disposed in parallel to a scanning direction of a line-shaped pulse laser irradiated upon the polycrystallization laser annealing (see for example column 6 lines 30-43).

Examiner takes official notice that it was well known to those skilled in the art at the time of the invention that the more similar the manufacturing conditions of semiconductor devices the more similar their properties will be. As evidence of this one can see for example *Knapp* column 2 lines 65-67 that states that transistors manufactured close to each other will have similar characteristics. As further evidence one can note the expansion of the Toyota Manufacturing system and statistical process control in general with its emphasis on reducing

manufacturing variation to a wide variety of manufacturing industries including semiconductor manufacturing.

Knapp and *Kato* are analogous art because they are from the same field of endeavor, which is thin film transistor based devices, and attempt to solve the same problem, which is to reduce the variability between thin film transistors.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to manufacture the transistors of *Knapp* with their channels aligned as disclosed by *Kato*. Thus *Knapp* and *Kato* disclose the claimed invention except for providing that at least part of both channel regions of the correction transistor and the driving transistor are located on the same line extending in a direction crossing the scanning direction of the pulse laser. It would have been obvious to one having ordinary skill in the art at the time the invention was made to so align the channel regions since it was known in the art that semiconductor devices formed under similar conditions, which includes the portions of the polycrystalline layer used for the channel regions of the two transistors being formed at the same time, exhibit similar properties. The suggestion/motivation would have been to provide advantages such as to provide better charge carrier mobility by reducing grain boundaries along the length of the channels (see for example *Kato* column 6 lines 42-43) or to make the transistors more similar (see for example *Knapp* column 2 lines 66-67).

As to **claim 14**, in addition to the rejection of claim 12 over *Knapp* and *Kato:*

Knapp and *Kato* disclose the claimed invention except for the channel region of the correction transistor having portions differing in channel width in the channel length direction thereof. It would have been obvious to one having ordinary skill in the art at the time the invention was made to vary the width since it was known in the art that open pixel area is desirable and that packing of multiple elements could be optimized by adjusting the size of portions of some elements.

2. **Claims 6, 7, and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,359,605 to *Knapp et al.* ("*Knapp*") in view of knowledge of one of ordinary skill in the art at the time of the invention.

As to **claim 6**, in addition to the rejection of claim 1 over *Knapp*, *Knapp* further discloses a data line (see for example Fig. 3 item 14) and a power source line (see for example Fig. 3 item 22) and that the device is arranged as a matrix (see for example column 1 line 6).

Knapp does not expressly disclose that the data line and the power source line extend in a vertical scanning direction, and the correction transistor is formed between the data line and the power source line.

Knapp discloses the claimed invention except for the data line and the power source line extending in a vertical scanning direction, and the correction

transistor formed between the data line and the power source line. It would have been obvious to one having ordinary skill in the art at the time the invention was made to so arrange the components disclosed, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

As to **claim 7**, in addition to the rejection of claim 6 over *Knapp*:

Knapp does not expressly disclose that the driving transistor is formed on a side opposite to the correction transistor with the power source line located in between.

Knapp discloses the claimed invention except for the driving transistor being formed on a side opposite to the correction transistor with the power source line located in between. It would have been obvious to one having ordinary skill in the art at the time the invention was made to so arrange the components disclosed, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

As to **claim 10**, in addition to the rejection of claim 1 over *Knapp*, *Knapp* further discloses that the correction transistor and the driving transistor are p-channel transistors (see for example column 8 lines 65-66), and the pulse voltage line changes from a high level to a low level after the selection transistor is turned off (see for example Fig. 3 item 28 labeled VS2 and column 7 lines 31-

36, which state that VS2 may be the next or previous row conductor line; noting that the row conductor lines provide a pulse voltage after the selection transistor is turned off).

Allowable Subject Matter

9. Claims 16-19 allowed.

10. Claims 2, 3, 8, 9 and 15 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

12. The following is a statement of reasons for the indication of allowable subject matter: In the case of claims 2 and 8 Examiner found no prior art with the recited structure operated according to the timing of transistor operation given. In the case of claims 3, 9 and 15-16 Examiner found no prior art with the recited structure.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert R. Rainey whose telephone number is (571) 270-3313. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RR/

AMARE MENGISTU
SUPERVISORY PATENT EXAMINER